Instruction manual

DATA I/O

Programming systems for tomorrow...today

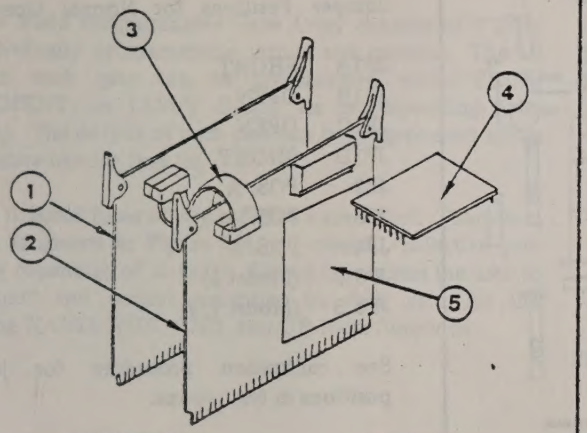
PROM PROGRAMMER
Program Card Set
909-1310-1

REV D JAN 79

025-1310-1

SECTION ONE

INSTALLATION AND OPERATION



1. Digital Card	701-1309
2. Analog Card	701-1310
3. Interconnect Cable	709-1608
4. Calib. Program Adapter	910-1310-1
5. Daughter Board	702-1327

Fig. 1-1. Program Card Set 909-1310-1.

DESCRIPTION

Program (Personality) Card Set 909-1310-1, with the appropriate Socket Adapter, provides Data I/O Programmers with the capability of programming and reading the Gate Arrays listed in Table 1-1. Socket Adapters are available for each Gate Array listed. Table 1-1 references the Socket Adapters required to program (or read) the Gate Arrays.

Program Card Set 909-1310-1 includes Calibrator Program Adapter 910-1310-1, which mates with Data I/O Universal Calibrator. As shipped, this Program Card Set is precalibrated according to Data I/O Calibration Procedure 017-1310-1, which is included in the Performance Check Section of this manual.

Table 1-1. FPGA types to Data I/O Socket Adapters.

Array Size	FPGA Part Number	Pinout	Socket Adapter
SIGNETICS			
16x9 FL	82S102	28 PIN	715-1227-5/9
16x9 FL	82S103	28 PIN	715-1227-5/9

CARD SET INSTALLATION

Turn Power OFF while changing Card Sets. Install the Daughter Board in J3 and J4 of the Analog Card. Install the Digital Card in programmer Brown-Orange card slot; install the interconnected Analog Card in White-White card slot. Component sides of cards should face forward in programmer Models 1-5 and down in programmer Models 7 and 9. Refer to the programmer manual for more detailed installation instructions.

SOCKET ADAPTER INSTALLATION

Models 1-5. Remove the original socket receptacle and 26-conductor cable from the programmer and replace it with the 715-1227-5 socket adapter/receptacle and 34-conductor cable. Orient the adapter with the pin 1 symbol at the top. Route the cable under the front panel and over the card cage, making sure that the red stripe is aligned with J2 pin 1 on the analog card.

Models 7/9. Hold the 715-1227-9 socket adapter perpendicular to the socket receptacle. Insert the two hook tabs into the upper slots in the receptacle, arranging the cable as shown in Figure 1-2 (b) - Swing the lower tabs into their slots, and slide the adapter toward the front of the programmer to lock it in place. Route the cable under the access door and into the opening.

Both Models. Connect the cable from the socket adapter to J2 on the analog card.

NOTE: The Gate Array Card Set functions in all Model 1-5 programmers. Do not use the Satellite. Model 7 and 9 programmers require Revision B Control Software. If the LOAD indicator remains ON when power is applied to the Model 7 or 9 programmer, the programmer will accommodate the Gate Array Card Set.

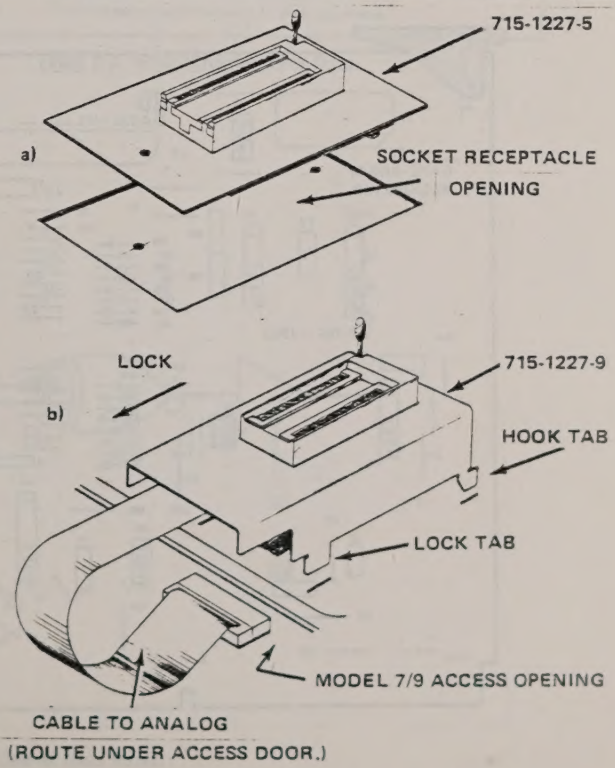
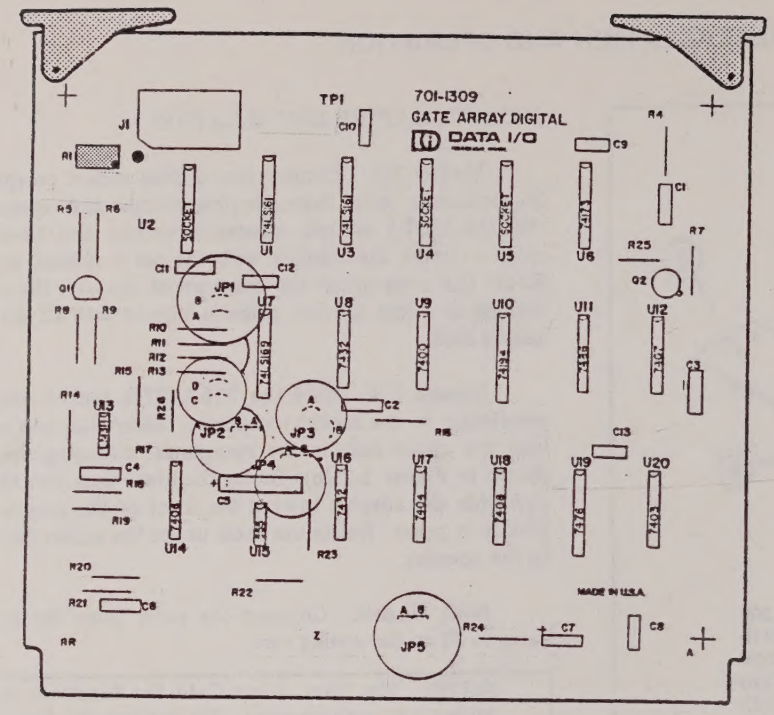


Figure 1-2. Gate Array Socket Adapter Installations in a) Model 5 and b) Model 7/9.



Jumper Positions for Normal Operations

JP1A	SHORT
JP1B	OPEN
JP1C	OPEN
JP1D	SHORT
JP2	POS. A
JP3	POS. A
JP4	POS. B
JP5A	(Model 5)
JP5 B	(Model 7/9)

See calibration procedure for jumper positions in test set-ups.

Adjustment locations on the Analog and Digital Cards are shown shaded.

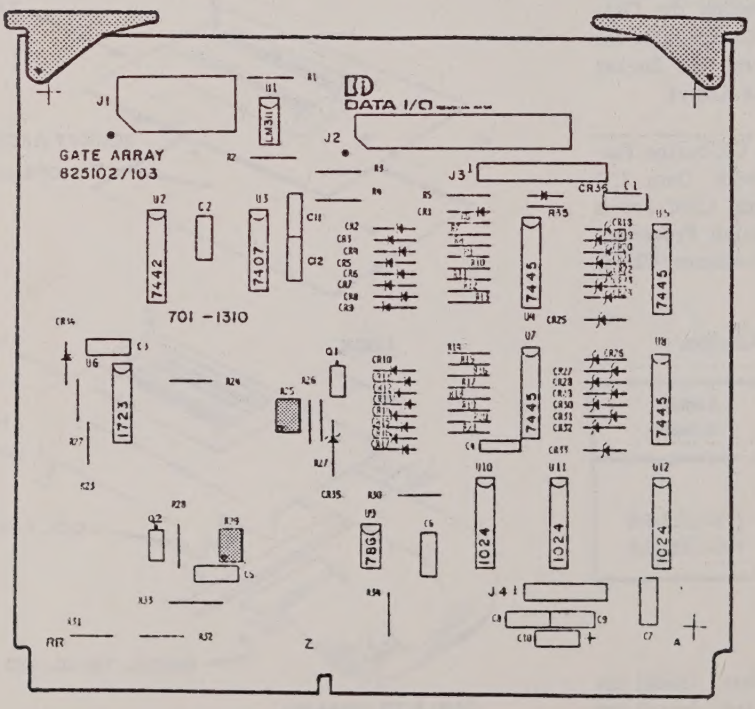


Figure 1-2. Jumper Positions and Adjustment Locations on the Analog and Digital Cards.

PROGRAMMING THE GATE ARRAY

INTRODUCTION

The Field Programmable Gate Array consists of 9 gates with individually programmable inputs and outputs. The 16 inputs to each gate can be programmed either TRUE, COMPLEMENT, or DON'T CARE via corresponding fuses (j) and (k). The output of each gate can be programmed active high or active low via fuse (s).

All internal fuses of virgin FPGA's are intact. Therefore, all fuses, as shown in Figure 1-3, are closed. Selective programming (opening) of links (j), (k) and (s) enables the user to assign input and output polarities to each gate for implementing NAND, NOR, AND, and OR logic functions.

PROGRAMMING CONSIDERATIONS

Output polarity for each gate is programmed before the inputs for that gate are programmed. For gate 1, the output polarity is programmed at word count (decimal) 000, then all sixteen input variables (I_0-I_{15} for gate 1) are programmed. I_0 is programmed at word count 000, I_1 is programmed at word count 001, I_2, at 002, etc. The output polarity for gate 2 is programmed at word count 16 as is input I_0. I_1 for gate 2 is programmed at 17, I_2 at 18, etc. The output polarity for gate 3 is programmed at word count 32, and so on. (See the Program Table, Figure 1-5).

PROGRAMMING OUTPUT POLARITY

Output polarity is defined by one of the data entries listed in Table 1-2.

Data is entered into the programmer in such a manner that bit 5 defines the output polarity and bits 1 and 2 define the state of input fuses. Bits 3, 4 and 6-8 are unused.

POLARITY	LOGIC FUNCTION	PROGRAM DATA HEX[1]	PROGRAM DATA OCTAL	FUSE STATE
Active Low	NAND	0X	00X	intact
Active High	AND	1X	02X	blown

NOTE: X denotes I_0 value to be programmed at the same word count.

Table 1-2. Output Programming Data.

PROGRAMMING INPUTS

The sixteen inputs for each output of the FPGA are programmed using low order bits 1 and 2 of the programmer RAM. Therefore, the choices for the right-most digit of data are 0, 1, 2, and 3 (Hex/Octal) as defined in Table 1-3.

DESIRED INPUT FUNCTION	PROGRAM DATA HEX[1]	PROGRAM DATA OCTAL[1]	FUSE STATES J	FUSE STATES K
Delete[2]	X0	0X0	intact	intact
Active Low	X1	0X1	blown	intact
Active High	X2	0X2	intact	blown
Don't Care	X3	0X3	blown	blown

NOTES: [1] X denotes output polarity (F0) if at word count where output is programmed. X = 0 at all other word counts.
[2] A single deleted input eliminates the entire output gate.

Table 1-3. Input Programming Data.

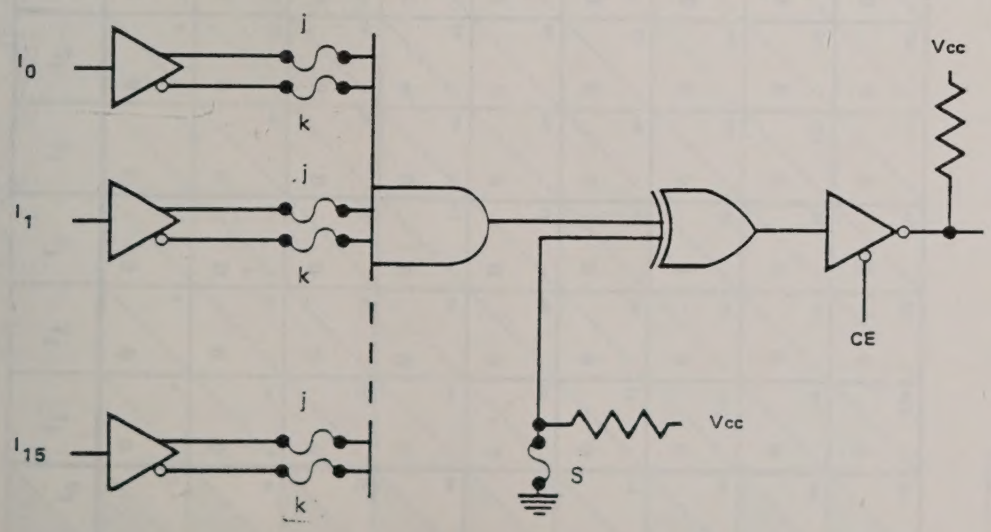


Figure 1-3. Equivalent Logic Path for One of Nine Gates.

FPGA PROGRAM TABLE

The FPGA PROGRAM TABLE (Figure 1-4) is designed to aid in formatting "state-of-the-fuse" information for entry into the programmer. Each horizontal row defines the output polarity and the state of the 16 inputs (I_0 -I_{15}) for one of the 9 gates. Each row is composed of 16 cells corresponding to 16 programmer word counts. The first cell in each row defines the output polarity and the I_o input polarity. The remaining cells in the row define the state of inputs I_1 through I_{15}.

Example: Following is one row of a program table filled out to define F_o as

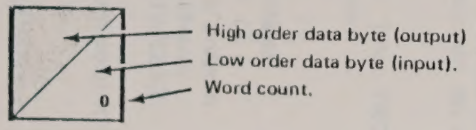
$$F_o = \overline{CE}\,(I_1 \cdot \overline{I_2} \cdot I_4 \cdot I_5 \cdot \overline{I_8} \cdot I_{14})$$

F_o / I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}
1 / 3	0 / 2	0 / 1	0 / 3	0 / 2	0 / 2	0 / 3	0 / 3	0 / 1	0 / 3	0 / 3	0 / 3	0 / 3	0 / 3	0 / 2	0 / 3
/ 16	0 / 17	0 /	0 /	0 /	0 /	0 /	0 / 23	0 / 24	0 / 25	0 /	0 /	0 / 28	0 / 29	0 / 30	0 / 31
														0 /	0 /

Figure 1-4. Sample FPGA Program Table

F_0 - F_9 / I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}
0	0 / 1	0 / 2	0 / 3	0 / 4	0 / 5	0 / 6	0 / 7	0 / 8	0 / 9	0 / 10	0 / 11	0 / 12	0 / 13	0 / 14	0 / 15
16	0 / 17	0 / 18	0 / 19	0 / 20	0 / 21	0 / 22	0 / 23	0 / 24	0 / 25	0 / 26	0 / 27	0 / 28	0 / 29	0 / 30	0 / 31
32	0 / 33	0 / 34	0 / 35	0 / 36	0 / 37	0 / 38	0 / 39	0 / 40	0 / 41	0 / 42	0 / 43	0 / 44	0 / 45	0 / 46	0 / 47
48	0 / 49	0 / 50	0 / 51	0 / 52	0 / 53	0 / 54	0 / 55	0 / 56	0 / 57	0 / 58	0 / 59	0 / 60	0 / 61	0 / 62	0 / 63
64	0 / 65	0 / 66	0 / 67	0 / 68	0 / 69	0 / 70	0 / 71	0 / 72	0 / 73	0 / 74	0 / 75	0 / 76	0 / 77	0 / 78	0 / 79
80	0 / 81	0 / 82	0 / 83	0 / 84	0 / 85	0 / 86	0 / 87	0 / 88	0 / 89	0 / 90	0 / 91	0 / 92	0 / 93	0 / 94	0 / 95
96	0 / 97	0 / 98	0 / 99	0 / 100	0 / 101	0 / 102	0 / 103	0 / 104	0 / 105	0 / 106	0 / 107	0 / 108	0 / 109	0 / 110	0 / 111
112	0 / 113	0 / 114	0 / 115	0 / 116	0 / 117	0 / 118	0 / 119	0 / 120	0 / 121	0 / 122	0 / 123	0 / 124	0 / 125	0 / 126	0 / 127
128	0 / 129	0 / 130	0 / 131	0 / 132	0 / 133	0 / 134	0 / 135	0 / 136	0 / 137	0 / 138	0 / 139	0 / 140	0 / 141	0 / 142	0 / 143

All numbers decimal.



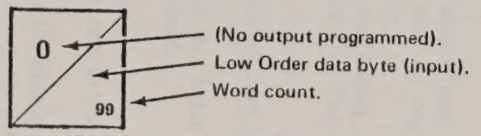


Figure 1-5. Sample FPGA Program Table.

SECTION TWO

CALIBRATION/PERFORMANCE CHECK

INTRODUCTION

Since PROM manufacturers' shipments can vary from lot-to-lot, slight variations in PROM programming yields are to be expected. However, each manufacturer usually specifies certain minimum PROM programming yields—provided that specific approved programming techniques are employed. Data I/O Programmers employ manufacturer-approved programming techniques: therefore, if programming yields diminish below PROM manufacturers' recommended minimums, or, if the program card set has been in use for more than ninety days since its last calibration, programmer performance should be checked as explained in this section.

The performance check includes calibration adjustments of program waveform amplitudes and includes go/no-go tests of all critical programming parameters. Also included in the performance check are tests on resistively loaded ac waveforms.

DATA I/O FIELD SERVICES

Data I/O Corp. furnishes complete programmer repair and calibration services at regional Field Service Centers and at the Data I/O factory. Contact your local Data I/O representative for further information.

TEST EQUIPMENT REQUIRED

To perform a complete performance check, the following equipment is required:

1. Data I/O Universal Calibrator, P/N 910-1071.

2. A. Prog. 1, 2, 3, 5: Data I/O Extender Card, P/N 910-1136.
   B. Prog. 9: Data I/O Extender Fixture, P/N 910-1074.

3. Digital Voltmeter: Fluke Model 8000A, or equivalent

4. Adjustment Tool: A three-inch screwdriver

5. Dual Trace Oscilloscope: Tektronix 465, or equivalent

6. Programmers 1, 2, 3, 5 only: Data I/O 13 inch Interconnect Cable, P/N 709-1613.

7. Programmer 9 only: Data I/O Interconnect Cables, P/N 709-1613 and 709-3412.

8. Jumper wires approximately 12 inches in length.

INSTALLATION OF UNIVERSAL CALIBRATOR

The following installation procedure assumes that the Universal Calibrator is mated with the Extender Card and that programmer power is off. On Programmers 1, 2, 3, and 5, remove the top cover to expose the card cage. To expose the card cage on the Model 9, open the access opening on the front of the chassis.

1. Remove end of 34-conductor cable from analog card. Remove both cards (analog and digital) from Programmer (or Satellite) card cage.

2. Remove end of 16-conductor cable from digital card J1.

CAUTION

Connector pins are fragile; careless connector extraction may result in bent or broken pins. Use a suitable tool--like a small screwdriver--when removing connectors from their sockets.

3. Install the extender card (with the Universal Calibrator in place).
   A. Programmers 1-5: Install the extender card into the analog card slot (white-white).
   B. Programmer 9: Install extender fixture into digital card slot (brown- orange).

4. A. Programmers 1-5: Install the analog card of the program card set into the card slot on top of the extender board. Refer to Figure 2-1.
   B. Programmer Model 9: Install the analog card in front card slot. Refer to Figure 2-2. The components should face the Calibrator.

5. A. Programmers 1-5: Install the digital card in the digital slot in the programmer.
   B. Programmer 9: Install the digital card behind the analog card on top of the extender card.

6. Making sure that cable red stripes and connector pins 1 are properly oriented, connect the analog card to the Universal Calibrator as follows:
   A. Connect J1 of the analog card to J1 of the Universal Calibrator using the strap between the analog and digital cards. Connect J2 of the analog card to J2 of the Universal Calibrator using the ribbon cable that connects the card set and the programmer.

7. Plug Calibrator Program Adapter into PROGRAM ADAPTER SOCKET on Universal Calibrator.

CAUTION

Be sure that the four-digit portions of both part numbers are identical: i.e. Analog card 701-XXXX is part of program card set 909-XXXX, which is calibrated by calibrator program adapter 910-XXXX.

8. Connect DVM ground probe to GND test point at left side of Universal Calibrator.

This completes installation of the Universal Calibrator.

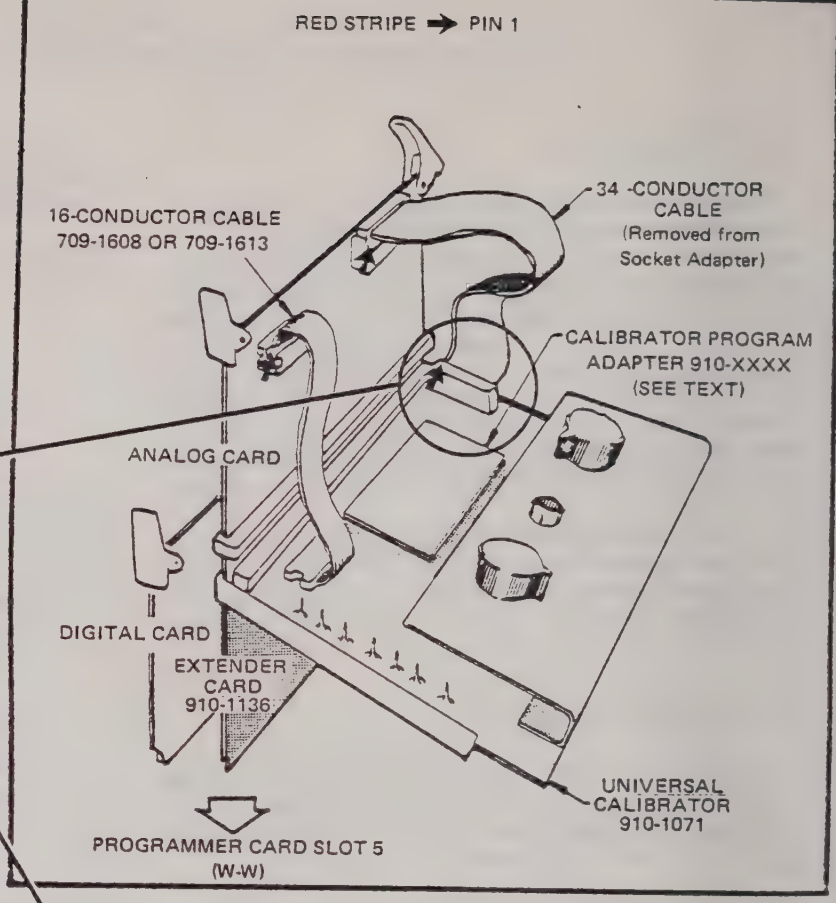


Figure 2-1. Installation of Universal Calibrator into Programmer Models 1, 2, 3, and 5 for Calibration/Performance Check.

NOTE: Attach the 34-conductor cable per notes on the calibration chart.

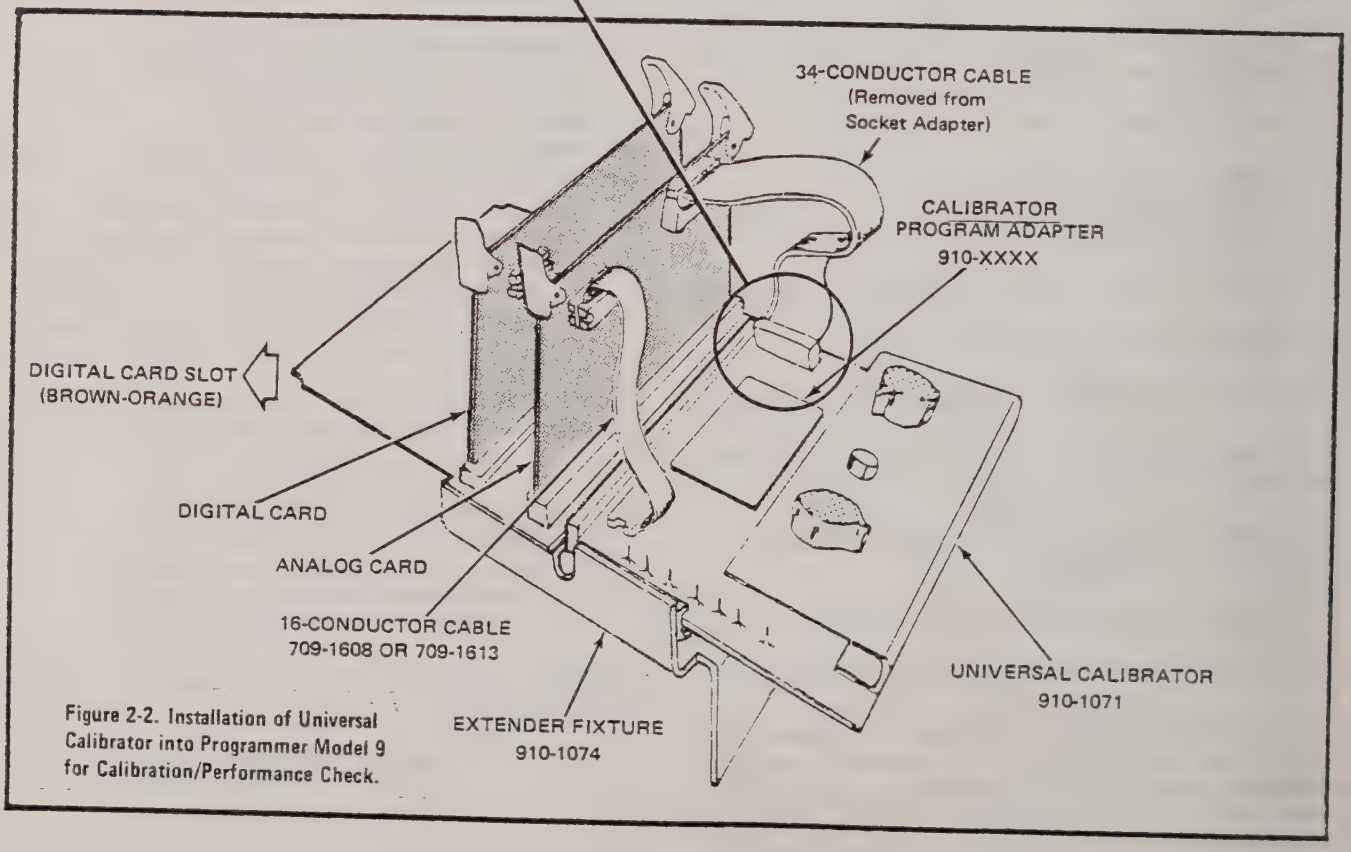


Figure 2-2. Installation of Universal Calibrator into Programmer Model 9 for Calibration/Performance Check.

CALIBRATION CHART

The calibration chart is to be used only with the (calibrator) program adapter specified in the title block of the chart.

The left-most portion of the chart contains truth tables for the calibrator program adapter. The truth tables are for documentation purposes only and have no bearing on the actual performance check/calibration procedures.

PROGRAMMER WORD COUNT COLUMN is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When using the chart, refer to the address (word count) corresponding to the address readout configuration of the programmer in use. For instance, if your programmer has a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static (DC steady state) conditions created by the Universal Calibrator may cause thermal damage to compo-components if Programmer is left unattended with advanced word count.

TEST DESCRIPTION column contains three kinds of tests: (1) power supplies, (2) performance checks, and (3) calibration adjustments. The power supply tests are contained in the first five rows of the chart. (Note that power supply adjustments are located in the programmer, not in the program card set.) Performance checks fill the bulk of the Calibration Chart; these are characterized by min/max voltage limits only. No nominal (NOM) values are given, and no adjustments (ADJ) are prescribed.

Calibration steps are those with entries in the ADJ and NOM columns. These steps are evident by the note "CALIBRATION STEP" in the comments column.

SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load select switch; S3 is the line select switch. Generally, each step on the Calibration Chart requires changing of switch positions. S1 is push to test, and should be held depressed only long enough to obtain a DVM reading.

CAUTION

DO NOT hold S1 depressed for extended periods. Certain measurements induce high programmer current levels. Extended hgih current operation (S1 depressed) may damage sensitive electronics components.

TEST POINT column gives test point location for DVM probe on Universal Calibrator. Some test points are located on the program card itself; for instance, if a test point is designated as U6 P8, it means that the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the comments column.

The ADJ column calls out potientiometer designations. The first four entries in the ADJ column refer to power supply potientiometers located on the power supply board of the Programmer. If adjustments are required, refer to Programmer manual. The remaining entries in the ADJ column refer to pots on the analog card. These are located as shown on page 1-2 in the Specifications section of this manual.

The LIMITS COLUMN is divided into three portions: MIN (minimum), NOM (Nominal), and MAX (Maximum). The values given are in volts, and indicate the range into which a given DVM reading should fall when S1 is pressed. If a reading is within the limits, no adjustment is required and the programmer (or program card set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (calibration steps), the card is non–functional and should not be used for programming.

NOTES are written in a block at the bottom of the calibration chart. These apply to certain calibration steps and are referenced by numbers in the comments column. Notes called out by letter in the comments column apply only to Model IX calibration.

PERFORMANCE CHECK AND CALIBRATION PROCEDURE

DC CALIBRATION

The following paragraphs describe the method by which a program card set is checked/calibrated in conjunction with the applicable Calibration Chart. The procedure assumes that the Universal Calibrator is properly installed, as previously described. The following procedure should be performed with the programmer in an ambient temperature range between 15°C to 35°C.

Initialization

1. Switch programmer power ON; allow programmer to warm up for approximately five minutes.
2. Programmers 1, 2, 3, and 5:
   Press: RESET
   RAM–RAM
   MANUAL
   PROGRAM
   START

   Programmer 9:
   Press: EXECUTE
   Set NORMAL/INVERT switch to INVERT.

Power Supply

During the procedure the programmer card cage should contain all boards normally used.

Connect DVM between GND and the Universal Calibrator test points given in Steps 1-1 through 1-5 on the Calibration Chart. Measured voltages should fall within the given limits. (Calibrator Switch positions do not matter.)

If any power supply voltage measurement reading is outside of the given range, adjustment must be made. Power supply adjustments are located on the power supply board within the programmer.

Performance Check/Calibration

1. Use FWD and REV keys on programmer keyboard to index the "address display" (word count) to the decimal (DEC), hexadecimal (HEX), or octal (OCT) address given in the word count column of the calibration chart.

CAUTION

DO NOT leave Word Count advanced beyond 000 for extended periods. Static (DC steady state) conditions created by the Universal Calibrator may cause thermal damage to components if programmer is left unattended with advanced word count. Press Reset to relieve possible thermal stresses.

2. With Word Count set, and DVM probes installed between GND and the indicated test point on the universal calibrator, set switches S2 and S3 to the positions indicated. Press S1 to test.

CAUTION

DO NOT hold S1 depressed for extended periods. Certain measurements induce high current levels within the Programmer. Extended high current operation (S1 depressed) puts unnecessary stress on sensitive electronic components.

3. While S1 is held, DVM readings should fall between the indicated limits for each measurement. If a DVM reading is outside of limits, or if the reading cannot be adjusted to fall within limits (ADJ column), DO NOT use the card set for programming.

Proceed through the Calibration Chart until all tests have been performed. At the conclusion of testing, turn programmer power OFF, and proceed to AC Dynamic Tests.

AC CALIBRATION

AC DYNAMIC TESTS

The following procedure is used to obtain the "Program Waveforms" shown on the Timing Diagram at the rear of this manual.

The waveforms at the inputs are on the first sheet and the outputs waveforms are on the second sheet.

These waveforms, indicated by circled digits (1, 2, 3...) on the timing diagram, are identically referenced on the Calibration Chart. The waveforms are obtained by selecting switch positions (S2 and S3) on the Universal Calibrator and feeding the selected signals to an appropriately triggered dual trace oscilloscope.

Test Set-Up

1. Make sure that programmer power is OFF.
2. A. Programmer 1-5: Remove the digital card from the card cage. Refer to Figure 2-3.
   B. Programmer 9: Remove the digital card from the extender. Refer to Figure 2-4.
3. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.
4. A. Programmers 1-5: Disconnect the other end of the 16-conductor cable from J1 of the analog card. Substitute the 13-inch cable supplied with the Calibrator, and connect J1 of the analog card to J1 of the digital card.
   B. Programmer 9: Connect the free end of the 16-conductor cable to digital card J1, assuring that cable red stripe and connector pin 1 are properly oriented.
5. Place the jumpers on the digital card in the following positions:
   A. Programmers 1-5: JP2 - Position A
      JP4 - Position B
      JP5 - Position A
   B. Programmer 9: JP2 - Position A
      JP4 - Position B
      JP5 - Position B
6. Connect triggered input channel of dual trace oscilloscope to digital card test pulse (TP1). Connect the other channel to TP3 on the Calibrator. Re-install the digital card per step 2, above.
7. Programmer 9: Set NORMAL/INVERT switch to NORMAL.
8. Turn Programmer power ON.
9. A. Programmers 1-5: Press RESET
      PROGRAM
      MANUAL
      ROM 2 - ROM 2
      START
      CLEAR

Depress and hold FWD key to observe following waveforms:

I_0

at Word Counts (Decimal) 00, 16, 32, 48, 64 80, 96, 112, 128. All other Word Counts ——10v

I_1

at Word Counts 01, 17, 33, 49, 65, 81, 97, 113, 129. All other Word Counts ———10v

I_{15}

at Word Counts 15, 31, 47, 63, 79, 95, 111, 127, 143. All other Word Counts ———10v

B. Programmer 9: Press: LOAD
EXECUTE
Observe

on all inputs
Deselect LOAD and Depress EXECUTE

I_0 ———— OV at Word Count (Decimal) 00, 16, 32, 48, 64, 80, 96, 112, 128. 10v at other Word Counts.

I_1 ———— OV at Word Count 01, 17, 33, 49, 65, 81, 97, 111, 127, 143. 10v at other Word Counts.

I_{15} ———— OV at Word Count 15, 31, 47, 63, 79, 95, 111, 127, 143. 10v at other Word Counts.

10. Press STOP and then turn the programmer power OFF. Slide the digital card out and place the jumpers in the following positions for the remaining waveform tests:

A. Programmers 1-5: JP2 Postion B
JP4 Postion A
JP5 Position A

B. Programmer 9: JP2 Postion B
JP4 Position A
JP5 Position B

Reinstall the digital card.

11. A. Programmer 5:
Press: RESET
PROGRAM
MANUAL
ROM 2 - ROM 2
START
FWD

Observe waveforms per Timing Diagram and Calibration Chart.

B. Programmer 9:
Press: LOAD
EXECUTE

Deselect LOAD, depress EXECUTE, then depress SET and FWD simultaneously. Word Count 000 waveforms may be observed.

For waveform observations at succeeding Word Counts, depress STOP, FWD then depress SET and FWD keys simultaneously.

The "Program Waveforms" on the timing diagram at the rear of the manual are cross-referenced to the "Test Description" column on the Calibration Chart by circled digits (①,②, ③,..). To obtain the various waveforms, use S2 and S3 on the Universal Calibrator to select the positions indicated in the "Switch Positions" column of the calibration chart and press S1 to test. S3 routes analog card output to TP3 (oscilloscipe probe); S2 selects resistive loads, which are connected to ground when S1 is pressed. NOTE: All other information on the calibration chart is of no importance during waveform observations.

CAUTION

When S1 is pressed, high currents are induced within the programmer; do not hold S1 depressed for extended periods. High currents are also present when the programmer is locked into program mode with advanced word count; RESET before leaving programmer unattended during these tests.

During these tests note that the Abort, Pause and Reject functions of the program card set remain active; Press WORD SKIP to refresh the display. The abort timer signals a reject after a specific programming time. The pause timer controls the on/off time of the programming time of the programming function. The position of the reject jumper (C or M) limits the number of applied programming pulses. Refer to the notes column of the timing diagram for definitions of the abort, pause, and reject functions.

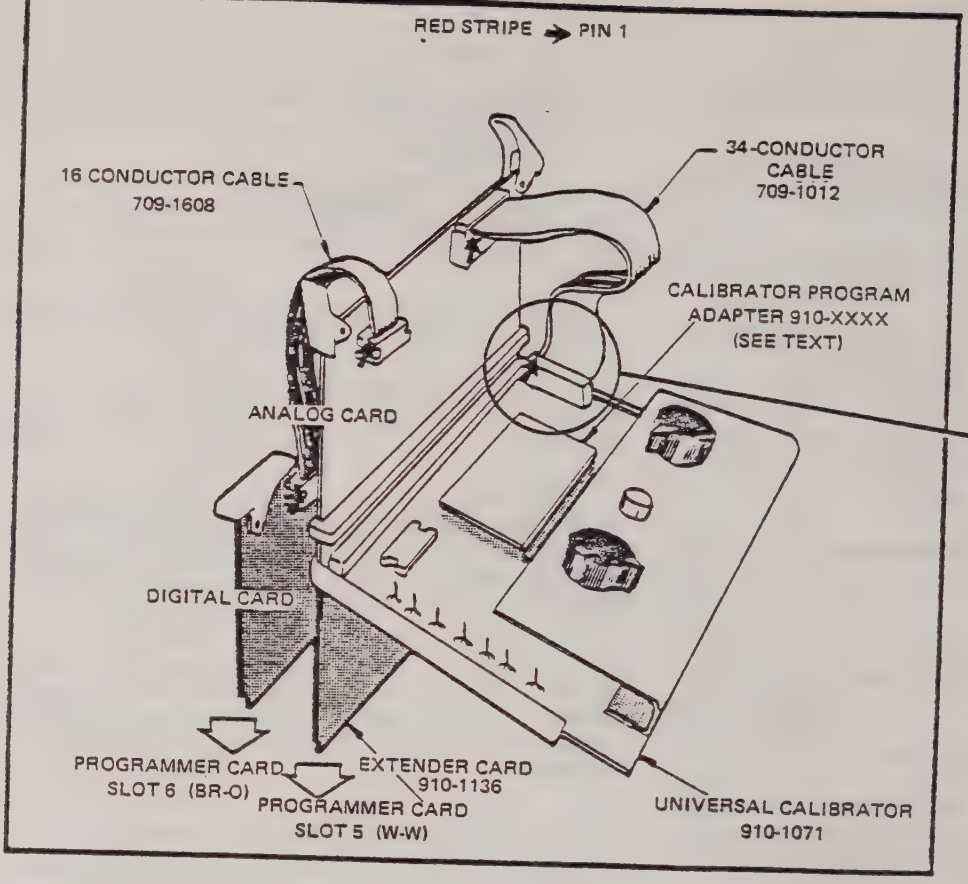
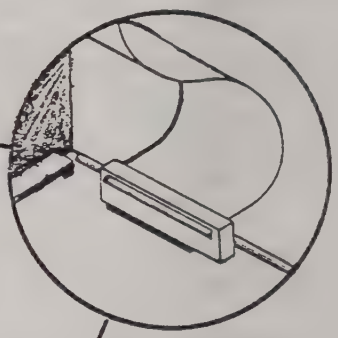


Figure 2-3. Installation of Universal Calibrator into Programmer Models 1, 2, 3, and 5 for AC Dynamic Tests.



NOTE: Attach the 34-conductor cable per notes on the calibration chart.

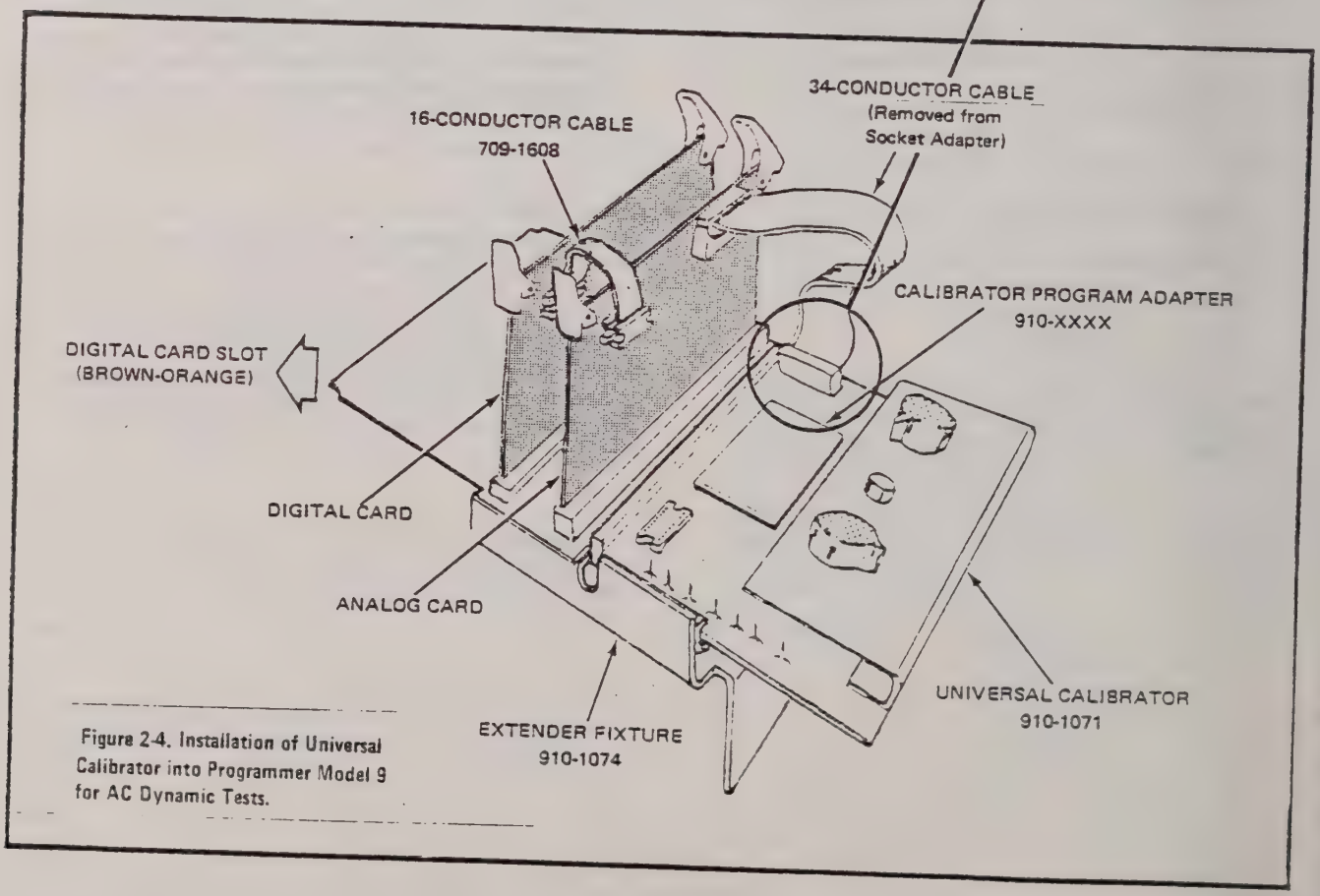


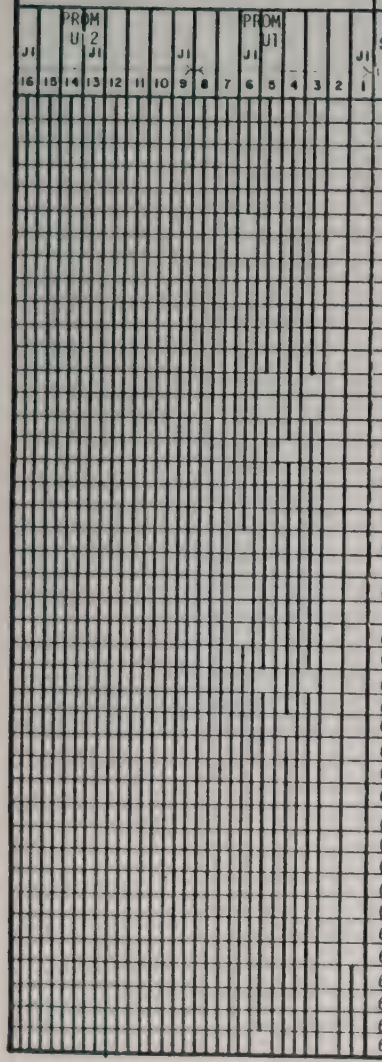
Figure 2-4. Installation of Universal Calibrator into Programmer Model 9 for AC Dynamic Tests.

DATA I/O
REDMOND, WASH.

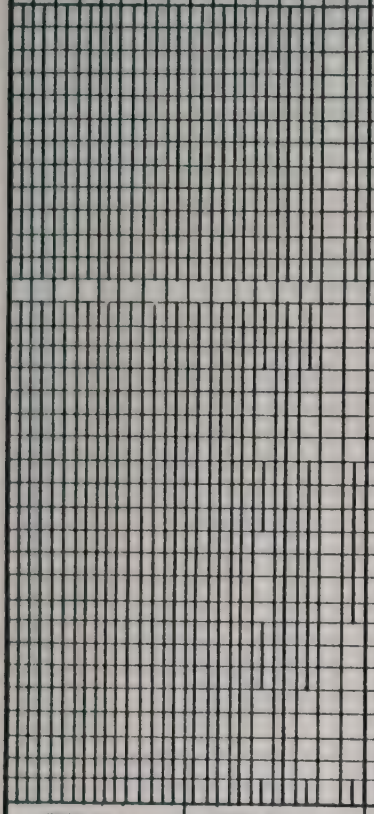
CALIBRATION CHART 017-1310-1
FIXTURE 702-1071
PROGRAM ADAPTER 910-1310-1
PROGRAM CARD 909-1310-1

MANUFACTURE SIGNETICS
PROM SIGNETICS GATE ARRAY

DATE	SYM	REVISION RECORD	DR	CK
2-16-78	A	RELEASE	DP	JK
	B	#2385		Dc
12-8	C	CN #2616	TC	



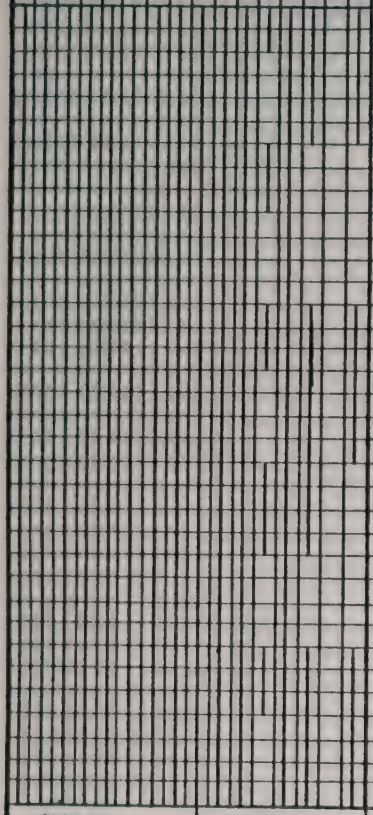
STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	TEST DESCRIPTION	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	PRESS S1	COMMENTS
1-1	000	00	000	+24			+24	R26	23.5	24.0	24.5		)
1-2	000	00	000	POWER +48			+48	R24	49.4	49.7	49.8		) ADJUSTMENTS ARE LOCATED ON THE POWER SUPPLY
1-3	000	00	000	SUPPLY + 5			+ 5	R18	5.05	5.1	5.15		) BOARD. SEE PROGRAMMER MANUAL.
1-4	000	00	000	- 9			- 9	R40	-8.8	-9.0	-9.2		)
1-5	000	00	000	PROGRAMMABLE SUPPLY			PROG V		14.0		17.0		)
2-1	001	01	001	VCC PROGRAM, V SET (2)	5	1	TP3	R25	8.5	8.75	9.0		NOTE: 34 PIN CABLE TO BE INSERTED FROM ANALOG
2-2	001	01	001	VCC PROGRAM, V REG	6	1	TP3		8.4		8.75		CONNECTOR J2 TO CONNECTOR J2 OF 910-1071
2-3	002	02	002	VCC VERIFY, V SET	5	1	TP3		4.75	5.0	5.25		CALIBRATOR. BE SURE THAT PIN 1 OF J2
2-4	002	02	002	VCC VERIFY, V REG	6	1	TP3		4.75		5.25		(26 PIN) ON CALIBRATOR MATCHES RED DOT
3-1	002	02	002	VOPF,FORCED OUTPUT V PROG FØ	4	11	TP3	R29	16.5	17.2	17.5		ON 34 PIN CABLE (PIN 1 TO PIN 1)
3-2	002	02	002	VOPF, REG - FØ	5	11	TP3		16.5		17.5		
3-3	002	02	002	IOPF LIMIT - FØ	6	11	TP3		5.5		7.5		DAUGHTER CARD 702-1327 MUST BE INSERTED
3-4	003	03	003	VOPF KILL - FØ	7	11	TP3		5.5		7.5		INTO 701-1310 BOARD FOR ALL TESTS.
4-1	003	03	003	VIX CE PROGRAM ENABLE LEVEL	3	10	J4-1		0.0		0.4	+	
5-1	004	04	004	CE VIH (3)	2	10	TP3		9.6		10.5		
5-2	005	05	005	CE VIL	10	10	TP3		2.6		3.6		+J4 PIN 1 TEST POINT IS LOC-
6-1	000	00	000	I/Ø VIL	10	20	TP3		0.0		0.4		ATED ON 702-1327 DAUGHTER
6-2	000	00	000	VIX, I1 DESELECT	7	19	TP3		0.0		0.4		BOARD.
6-3	000	00	000	I1 PULL-UP TEST	3	19	TP3		9.6		10.5		
6-4	001	01	001	I0,I2-I15 PULL-UP TESTS	3	2-9,20, 13-18	TP3		5.5		6.5		15 TESTS
6-5	001	01	001	VIX, I0,I2-I15 DESLEECTS	7	2-9,20, 13-18	TP3		5.5		6.5		15 TESTS
6-6	001	01	001	I1 VIL	10	19	TP3		9.6		10.5		
6-7	002	02	002	I2 VIL	10	18	TP3		0.0		0.4		
6-8	003	03	003	I3 VIL	10	17	TP3		0.0		0.4		
6-9	004	04	004	I4 VIL	10	16	TP3		0.0		0.4		
6-10	005	05	005	I5 VIL	10	15	TP3		0.0		0.4		
6-11	006	06	006	I6 VIL	10	14	TP3		0.0		0.4		
6-12	007	07	007	I7 VIL	10	13	TP3		0.0		0.4		
6-13	008	08	010	I8 VIL	10	2	TP3		0.0		0.4		
6-14	009	09	011	I9 VIL	10	3	TP3		0.0		0.4		
6-15	010	0A	012	I10 VIL	10	4	TP3		0.0		0.4		
6-16	011	0B	013	I11 VIL	10	5	TP3		0.0		0.4		
6-17	012	0C	014	I12 VIL	10	6	TP3		0.0		0.4		
6-18	013	0D	015	I13 VIL	10	7	TP3		0.0		0.4		
6-19	014	0E	016	I14 VIL	10	8	TP3		0.0		0.4		
6-20	015	0F	017	I15 VIL	10	9	TP3		0.0		0.4		
6-21	016	10	020	IØ VIH (1)	2	20	TP3		4.5		5.5		
6-22	017	11	021	I1 VIH	2	19	TP3		4.5		5.5		
6-23	018	12	022	I2 VIH	2	18	TP3		4.5		5.5		
6-24	019	13	023	I3 VIH	2	17	TP3		4.5		5.5		



STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	TEST DESCRIPTION	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	CALIBRATION CHART 017-1310-1 (CONTINUED) PAGE 2 OF 4 COMMENTS
6-25	020	14	024	I4 VIH	2	16	TP3		4.5		5.5	
6-26	021	15	025	I5 VIH	2	15	TP3		4.5		5.5	
6-27	022	16	026	I6 VIH	2	14	TP3		4.5		5.5	
6-28	023	17	027	I7 VIH	2	13	TP3		4.5		5.5	
6-29	024	18	030	I8 VIH	2	2	TP3		4.5		5.5	
6-30	025	19	031	I9 VIH	2	3	TP3		4.5		5.5	
6-31	026	1A	032	I10 VIH	2	4	TP3		4.5		5.5	
6-32	027	1B	033	I11 VIH	2	5	TP3		4.5		5.5	
6-33	028	1C	034	I12 VIH	2	6	TP3		4.5		5.5	
6-34	029	1D	035	I13 VIH	2	7	TP3		4.5		5.5	
6-35	030	1E	036	I14 VIH	2	8	TP3		4.5		5.5	
6-36	031	1F	037	I15 VIH	2	9	TP3		4.5		5.5	
7-1				SET UP								REMOVE 34 PIN CABLE FROM CALIBRATOR J2, INSERT THIS END INTO CALIBRATOR J2 AT REAR OF
8-1	002	02	002	F0 VOP (4)	5	7	TP3		16.5		17.5	
8-2	002	02	002	FX DESELECT (5)	7	8-10, 17-21	TP3		4.9		5.15	8 TESTS 26 PIN CONNECTOR, PIN 5 OF CABLE MUST MATCH PIN 1 OF CALIBRATOR J2.
8-3	003	03	003	F0 VOH	2	7	TP3		3.0		3.4	
8-4	003	03	003	F0 VOL	4	7	TP3		0.0		0.6	
8-5	003	03	003	F0 VOL READ	4	7	R1		0.0		0.4	*
8-6	003	03	003	F0 VOH READ	2	7	R1		4.9		5.15	*
8-7	018	12	022	F1 VOP	5	8	TP3		16.5		17.5	
8-8	018	12	022	FX DESELECT	7	7 9,10 17-21	TP3		4.9		5.15	8 TESTS
8-9	019	13	023	F1 VOH	2	8	TP3		3.0		3.4	
8-10	019	13	023	F1 VOL	4	8	TP3		0.0		0.6	
8-11	019	13	023	F1 VOL READ	4	8	R1		0.0		0.4	*
8-12	019	13	023	F1 VOH READ	2	8	R1		4.9		5.15	*
8-13	034	22	042	F2 VOP	5	9	TP3		16.5		17.5	
8-14	034	22	042	FX DESELECT	7	7,8,10, 17-21	TP3		4.9		5.15	8 TESTS
8-15	035	23	043	F2 VOH	2	9	TP3		3.0		3.4	
8-16	035	23	043	F2 VOL	4	9	TP3		0.0		0.6	
8-17	035	23	043	F2 VOL READ	4	9	R1		0.0		0.4	*
8-18	035	23	043	F2 VOH READ	2	9	R1		4.9		5.15	*
8-19	050	32	062	F3 VOP	5	10	TP3		16.5		17.5	

*NOTE: R1 TEST POINT, MEASURE LEFT SIDE OF R1 ON 701-1310.

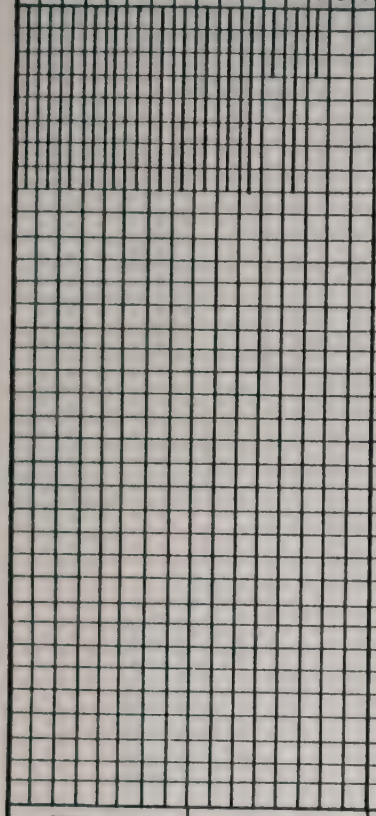
PROM U2 TRUTH TABLE	PROM U1 TRUTH TABLE
LINE =HI(1)	NO LINE=LOW(0)



STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	TEST DESCRIPTION	SWITCH POSITIONS S2	S3	MEASUREMENT PRESS S 1 TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	CALIBRATION CHART 017-1310-1 (CONTINUED) PAGE 3 of 4 COMMENTS
8-20	050	32	062	FX DESELECT	7	7-9, 17-21	TP3		4.9		5.15	8 TESTS
8-21	051	33	063	F3 VOH	2	10	TP3		3.0		3.4	
8-22	051	33	063	F3 VOL	4	10	TP3		0.0		0.6	
8-23	051	33	063	F3 VOL READ	4	10	R1		0.0		0.4	*
8-24	051	33	063	F3 VOH READ	2	10	R1		4.9		5.15	*
8-25	066	42	102	F4 VOP	5	21	TP3		16.5		17.5	
8-26	066	42	102	FX DESELECT	7	7-10, 17-20	TP3		4.9		5.15	8 TESTS
8-27	067	43	103	F4 VOH	2	21	TP3		3.0		3.4	
8-28	067	43	103	F4 VOL	4	21	TP3		0.0		0.6	
8-29	067	43	103	F4 VOL READ	4	21	R1		0.0		0.4	*
8-30	067	43	103	F4 VOH READ	2	21	R1		4.9		5.15	*
8-31	082	52	122	F5 VOP	5	20	TP3		16.5		17.5	
8-32	082	52	122	FX DESELECT	7	7-10,21, 17-19	TP3		4.9		5.15	8 TESTS
8-33	083	53	123	F5 VOH	2	20	TP3		3.0		3.4	
8-34	083	53	123	F5 VOL	4	20	TP3		0.0		0.6	
8-35	083	53	123	F5 VOL READ	4	20	R1		0.0		0.4	*
8-36	083	53	123	F5 VOH READ	2	20	R1		4.9		5.15	*
8-37	098	62	142	F6 VOP	5	19	TP3		16.5		17.5	
8-38	098	62	142	FX DESELECT	7	7-10,17, 18,20, 21	TP3		4.9		5.15	8 TESTS
8-39	099	63	143	F6 VOH	2	19	TP3		3.0		3.4	
8-40	099	63	143	F6 VOL	4	19	TP3		0.0		0.6	
8-41	099	63	143	F6 VOL READ	4	19	R1		0.0		0.4	*
8-42	099	63	143	F6 VOH READ	2	19	R1		4.9		5.15	*
8-43	114	72	162	F7 VOP	5	18	TP3		16.5		17.5	
8-44	114	72	162	FX DESELECT	7	7-10,17, 19,21	TP3		4.9		5.15	8 TESTS
8-45	115	73	163	F7 VOH	2	18	TP3		3.0		3.4	
8-46	115	73	163	F7 VOL	4	18	TP3		0.0		0.6	
8-47	115	73	163	F7 VOL READ	4	18	R1		0.0		0.4	*
8-48	115	73	163	F7 VOH READ	2	18	R1		4.9		5.15	*

* NOTE: R1 TEST POINT, MEASURE LEFT SIDE OF R1 ON 701-1310.

PROM U2 TRUTH TABLE	PROM U1 TRUTH TABLE
LINE = HI (1)	NO LINE = LOW(0)



STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	TEST DESCRIPTION	SWITCH POSITIONS S2	S3	MEASUREMENT PRESS S 1 TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	COMMENTS
8-49	130	82	202	F8 VOP	5	17	TP3		16.5		17.5	
8-50	130	82	202	FX DESELECT	7	7-10, 18-21	TP3		4.9		5.15	8 TESTS
8-51	131	83	203	F8 VOH	2	17	TP3		3.0		3.4	
8-52	131	83	203	F8 VOL	4	17	TP3		0.0		0.6	
8-53	131	83	203	F8 VOL READ	4	17	R1		0.0		0.4	*
8-54	131	83	203	F8 VOH READ	2	17	R1		4.9		5.15	*
9-1	131	83	203	GND TEST	8	22	TP3		0.0		0.08	

*NOTE: R1 TEST POINT, MEASURE LEFT SIDE OF R1 ON 701-1310.

PROM U2 TRUTH TABLE	PROM U1 TRUTH TABLE
LINE = HI(1)	NO LINE=LOW(0)

SECTION FOUR
CIRCUIT DESCRIPTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the programmer and with each other. The analog card interfaces with the FPGA being programmed. Figure 4-1 gives a generalized block diagram of the relations among the cards, the programmer, and the FPGA being programmed or read.

DIGITAL CARD

The digital card receives data from the programmer on the DI Bus, and from the FPGA on the DO Bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command FPGA program pulses from the analog card until either ABORT or REJECT is signaled, or until the bit is programmed.

ANALOG CARD

The analog card receives bit addresses, word addresses, timing, and mode commands. Analog card output consists of FPGA manufacturer's specified programming voltages and currents. When specified by the manufacturer, each programmed FPGA bit is tested for loading and/or leakage. Following the program cycle, FPGAs are read by the analog card to verify that programmed data matches truth table data.

DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow and timing. Detailed cicuit schematics with timing diagrams and truth tables are found at the rear of this manual.

DIGITAL CARD CIRCUIT DESCRIPTION

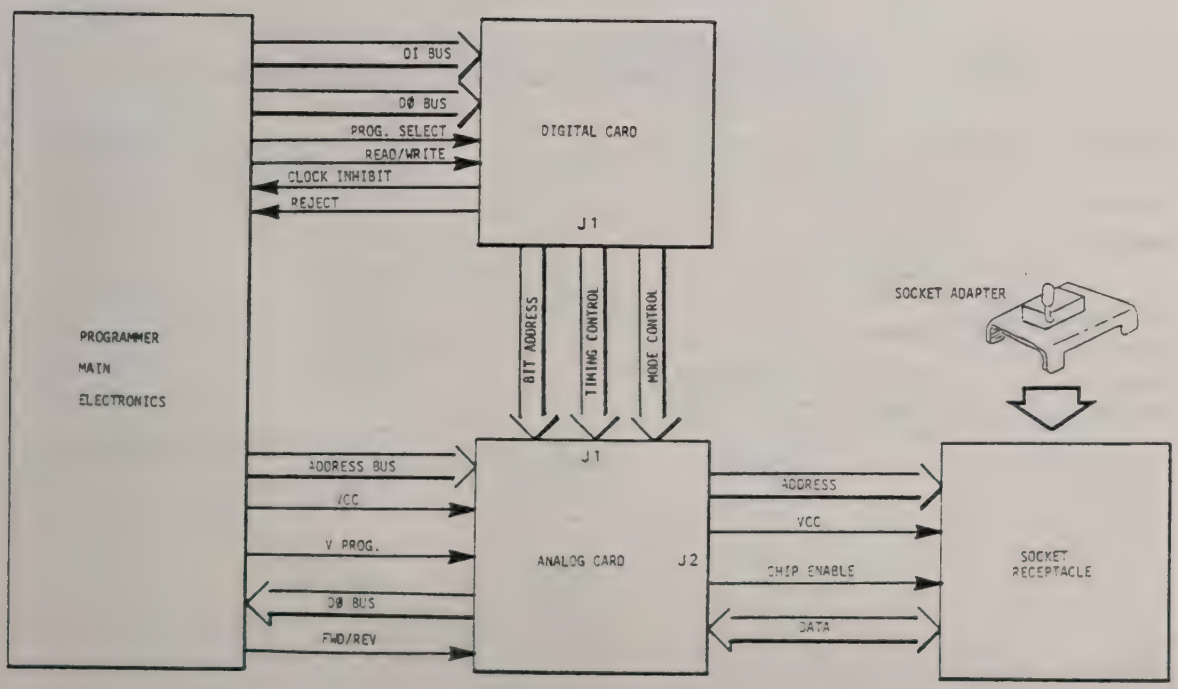
BLOCK DIAGRAM

Figure 4-2 is generalized block diagram of the digital card. This diagram shows signal flow and functional relationships, but does not include detailed interconnect information. Refer to the schematics and timing diagrams (with truth tables) at the rear of this manual for details of circuit connection and operation. The following paragraphs discuss the functions of the digital card.

PROGRAM MEMORY

When the digital card is selected for operation, the Program Memory will set upon receiving a WRITE command. Program Memory will also set on BUSY TEST (JP5-A, Programmer 5) or READ (JP5-B Programmer 9). When the Program Memory sets, the programmer clock is halted and RESET is removed from the Mode Controller and the Timing Sequencer.

Figure 4.1. Simplified Block Diagram of Program Card Set.



CLOCK GENERATOR

The clock generator is a two-speed, free running clock. The slower of the two speeds is selected by either a WRITE pulse or by a signal from the Timing Sequencer. Clock pulses are applied to the Mode Controller, the Timing Sequencer, the DI and DO Registers, the Abort Counter, and the Invert Memory.

TIMING SEQUENCER

The Timing Sequencer consists of a 4-bit counter which drives a 32x8 Timing PROM. This combination generates timing signals for analog control, bit test, Abort Counter increment, and clock speed control.

ABORT COUNTER/TIMER

The digital card contains both an Abort Counter and an Abort Timer. If the Abort Counter is selected (JP3 in position A), the number of programmming attempts (defined by JP1-A, B, C, D) is loaded into the counter and counted down. After the preset number of programming attempts have been made, the Abort Count will flag an abort condition.

If the Abort Timer is selected (JP3 in position B), the analog card is given a preset length of time to successfully program a fuse. If the fuse should fail to program during the preset time interval, the timer will flag an abort condition.

MODE CONTROLLER

The Mode Controller consists of a 4-bit counter and two 32x8 PROMs. Outputs of the Mode Controller PROMs are used to steer data within the digital card, reset Program Memory, tests for Abort, test output data, etc. For a fuller understanding of the Mode Controller and its operation, refer to the schematic and truth tables.

ANALOG CARD CIRCUIT DESCRIPTION

ANALOG CARD OPERATION

The analog card receives control signals from the digital card via J1, and from the Programmer via card edge contacts. Figure 4-3 shows signal flow from the analog card components to the Gate Array being programmed. Refer to the truth tables and timing diagrams at the rear of this manual for precise details about signal amplitudes and timing relationships.

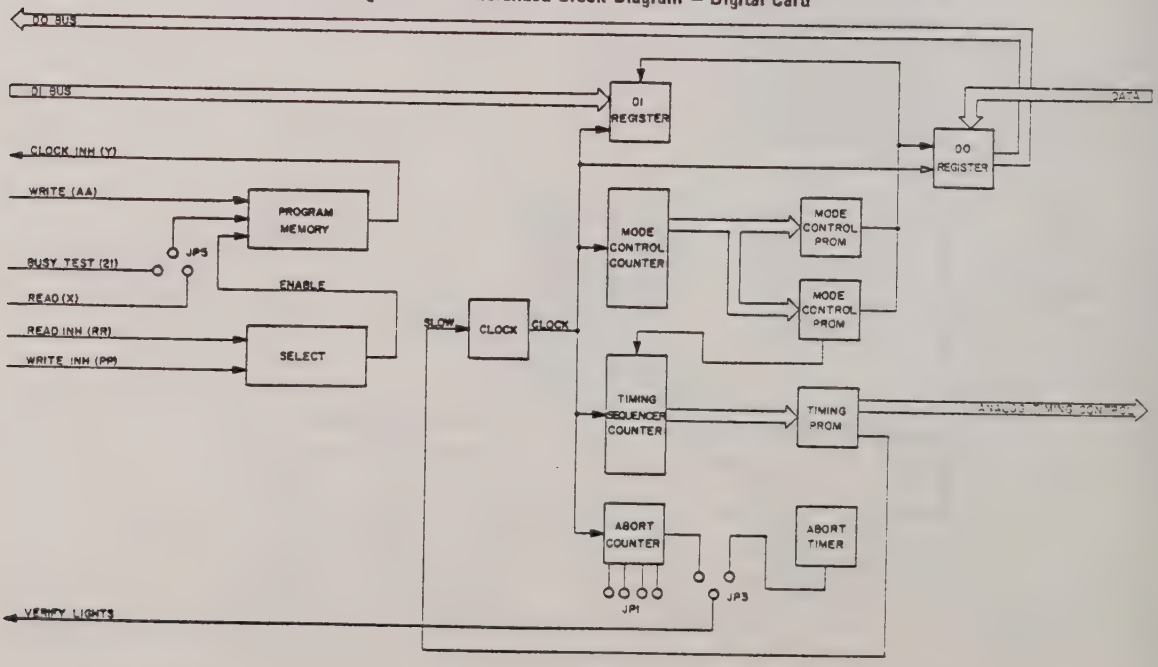
Each Gate Array fuse is programmed individually. An output polarity fuse is programmed, and then the associated input variable fuses are individually programmed. Address information presented to the card edge connectors, and information arriving from the digital card at J1 is used to select the appropriate fuse to read a program.

During the appropriate clock periods of the program cycle (see timing diagram) the output switches (Q1-19) are turned on allowing the output of the Program Voltage Generator to reach the device to be programmed.

PROGRAM VOLTAGE GENERATOR

The Program Voltage Generator is a current limited regulator which supplies the programming voltage to the Gate Array. The Program Voltage Generator is turned on and off by the digital card via J1-5 and U3.

Figure 4-2. Generalized Block Diagram — Digital Card



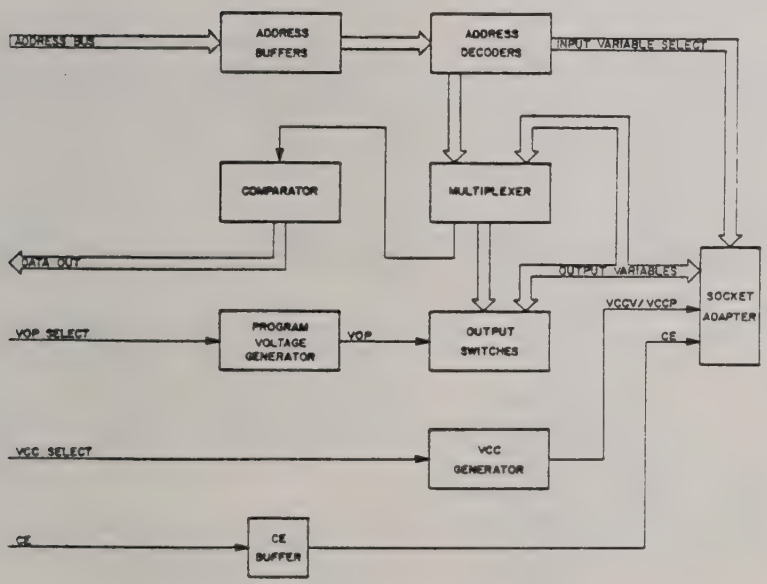
Vcc GENERATOR

The Vcc Generator is a current limited regulator with two selectable states: Vcc verify/read (VCCV) and Vcc program (VCCP). Vcc verify/read is applied to the device at all times other than when programming at which time Vcc program is selected. Vcc selection is made by the digital card via J1-6 and U3.

COMPARATOR

Any one of the nine Gate Array outputs may be selected by multiplexer U2 and presented to the Comparator U1. Here the output level is compared against the threshold derived by voltage divider R3-R2. The output of the comparator is in turn fed to the digital card, via J1-13, for processing.

Figure 4-3. Generalized Block Diagram – Analog Card.



Warranty

Data I/O equipment is guaranteed against defects in materials and workmanship. The warranty period is ninety days on new equipment, and thirty days on used equipment. Warranty period begins on receipt of equipment. Data I/O will repair or replace, at Data I/O's option, any equipment found to be defective within the warranty period.

Warranty service will be provided by Data I/O within a reasonable amount of time after notification by the purchaser to Data I/O of equipment malfunction. This service shall not apply to equipment that has been subjected to abuse, misuse, negligence or accident as determined by Data I/O, or to which any modifications, alterations, or attachments have been made without written authorization from Data I/O, nor shall it apply if the equipment is installed or operated in an environment containing excessive dirt, dust, moisture, fumes, humidity, or extremes of temperature.

This warranty policy is in lieu of all other warranties, expressed or implied, unless standard warranty exceptions are granted by Data I/O in writing.

Service

After expiration of the warranty period, service and repairs are billed at standard hourly rates, plus expenses, portal-to-portal. Time and one-half rate will apply outside of normal working hours.

Cost of engineering (where applicable) and parts, plus the cost of installation is billed at standard service labor rates when implementing approved, customer requested modifications.

Shipment

Products returned to Data I/O should be accompanied by a letter or enclosure explaining the reason for their return and action requested of Data I/O. Please include the following additional information: Company name and address; attention of; method of shipment desired; serial number; date of purchase; billing information, and purchase order number.

All products returned to Data I/O must be sent prepaid F.O.B. The warranty is voided if returned items are not packaged by the customer in original packing material, or in other Data I/O approved containers. If reshipment method is not specified by customer, Data I/O will return products by most expedient shipping method, F.O.B. our plant.

Ship returned equipment to:

DATA I/O CORPORATION
1297 N.W. Mall
Issaquah, Washington 98027

From Europe:

DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

Parts Ordering

Orders for parts should contain the following information:

a. Description of part(s) and Data I/O part number(s).
b. Quantity of each item to be ordered.
c. Equipment serial number and model number.
d. Corporate name of firm.
e. Shipping address of firm, including zip code.
f. Full name of person ordering the part(s).
g. To whose attention the part(s) are to be shipped.
h. Billing information.
i. Purchase order number.
j. Method of shipment.

Please send all parts orders to:

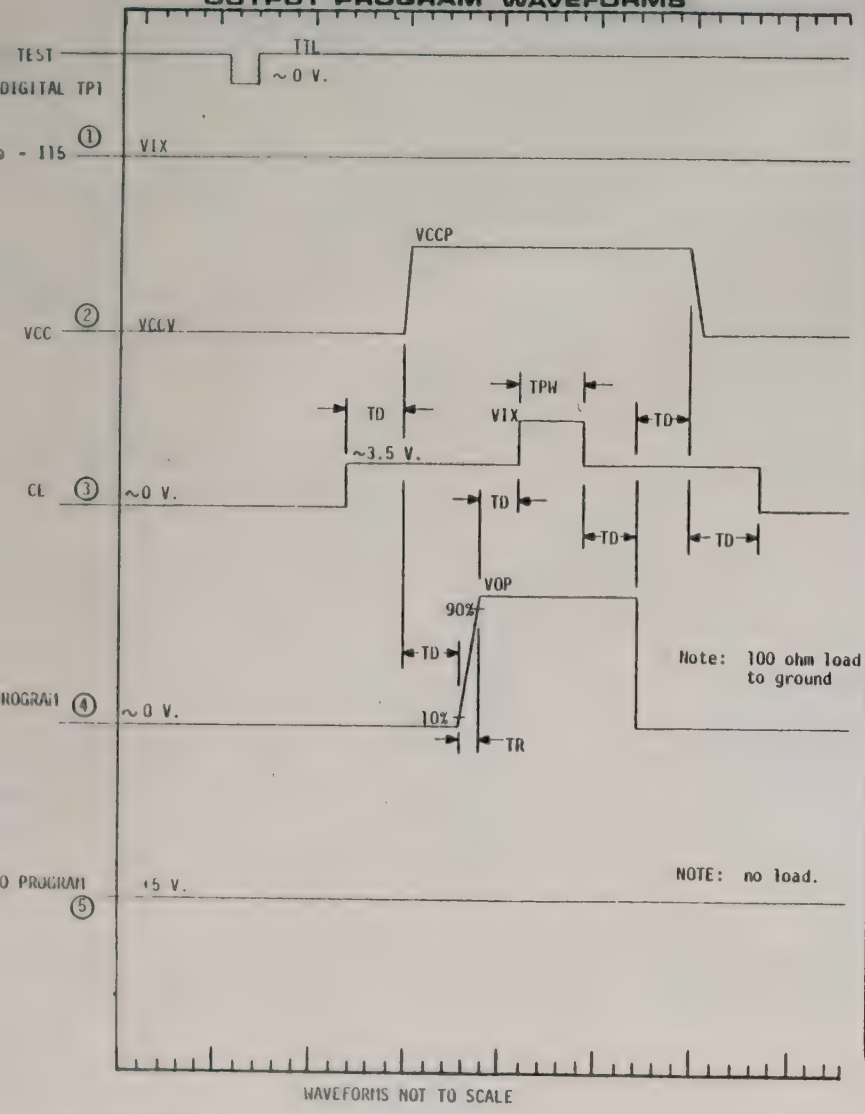
DATA I/O CORPORATION
P O Box 308
Issaquah, Washington 98027

From Europe:

DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

	DATE	SYM	REVISION RECORD	DR	CK
3	77	A	RELEASE		
11	77	B	UPDATED		
15MAR	78	–	REDRAWN (CONTINUED)	VZ	

OUTPUT PROGRAM WAVEFORMS



NOTES

WAVEFORM VARIABLES

VCCV	=	5.0 ± 0.25 V.
VCCP	=	8.75 ± 0.25 V.
VOP	=	17.0 ± 1.0 V.
VIX	=	10.0 ± 0.5 V.
TPW	=	1.25 ± 0.25 ms.
TR	=	10 to 50 us.
TD	≥	10 us
VIH	=	5.0 ± 0.5 V.

ABORT = 3 PULSE

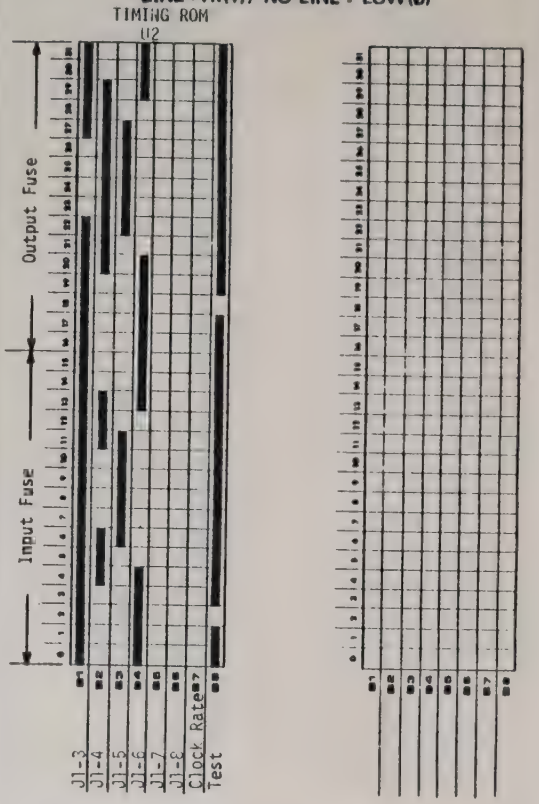
JUMPER POSITIONS

JP1 A = SHORT
JP1 B = OPEN
JP1 C = OPEN
JP1 D = SHORT
JP2 = POS. A
JP3 = POS. A
JP4 = POS. B
JP5 = POS. A (Programmers 1,5)
= POS. B (Programmer 9)

NOTE: FOR TEST ONLY, INSTALL JP2 TO POSITION B. THIS ENABLES THE CARD SET TO ALWAYS LOCK INTO PROGRAM.

TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)



DATA I/O ISSAQUAH, WASH.

SIGNETICS GATE ARRAY

DRAWN BY G. J.

APPROVED BY

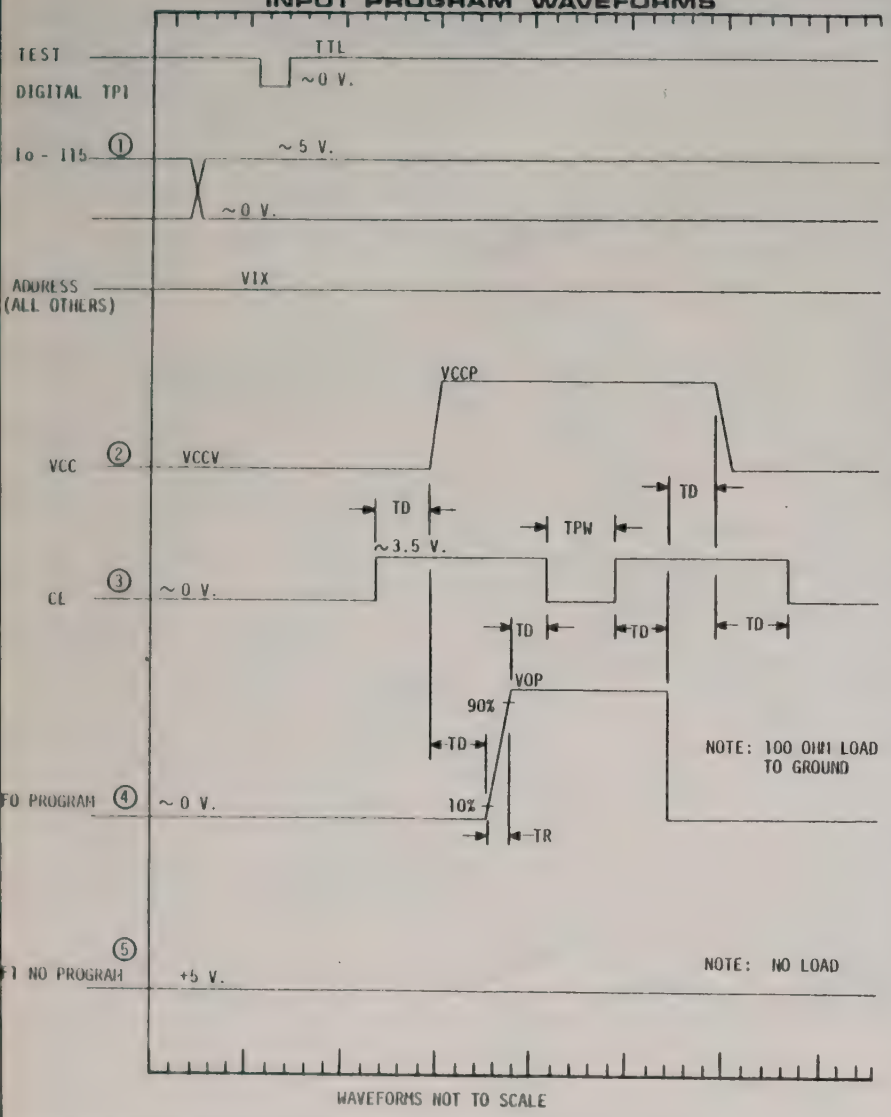
TITLE TIMING DIAGRAM Sheet 1 of 2

DATE 3-1-77

DRAWING NUMBER 007-1310-1

DATE	SYM	REVISION RECORD	DR	CK
9/78	C	ECN# 2385	DB	DG
9/78	-	ECR# 2425	KT	DB

INPUT PROGRAM WAVEFORMS



WAVEFORMS NOT TO SCALE

NOTES

WAVEFORM VARIABLES

VCCV	=	5.0 ± 0.25 V
VCCP	=	8.75 ± 0.25 V
VOP	=	17.0 ± 1.0 V
VIX	=	10.0 ± 0.5 V
TPW	=	1.25 ± 0.25 ms
TR	=	10 to 50 us
TD	≥	10 us
VIH	=	5.0 ± 0.5 V

ABORT = 3 PULSE

JUMPER POSITIONS

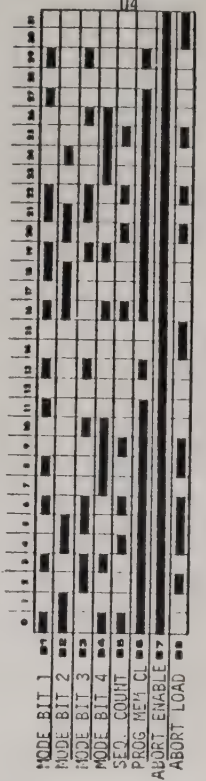
JP1 A	=	SHORT
JP1 B	=	OPEN
JP1 C	=	OPEN
JP1 D	=	SHORT
JP2	=	POS. A
JP3	=	POS. A
JP4	=	POS. B
JP5	=	POS. A (Programmers 1, 5)
	=	POS. B (Programmer 9)

NOTE: FOR TEST ONLY, INSTALL JP2 to POSITION B. THIS ENABLES THE CARD SET TO ALWAYS LOCK INTO PROGRAM.

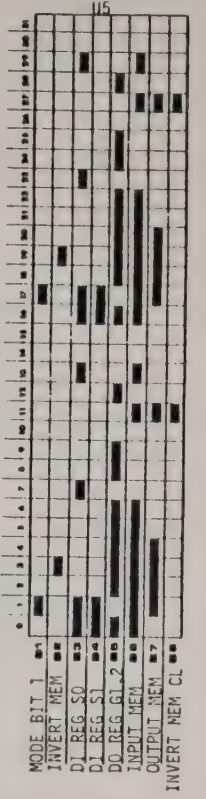
TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)

CONTROL ROM U4

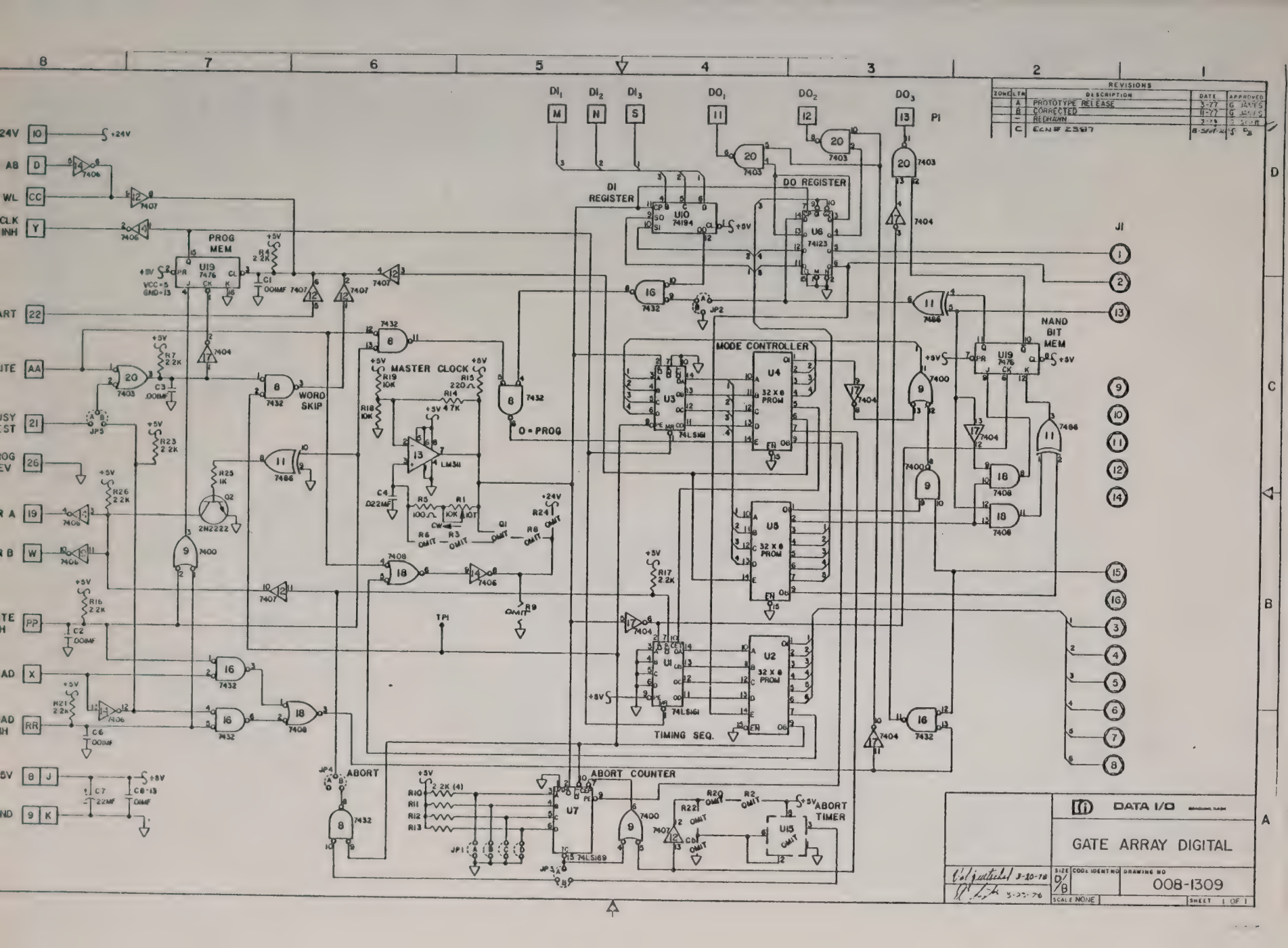


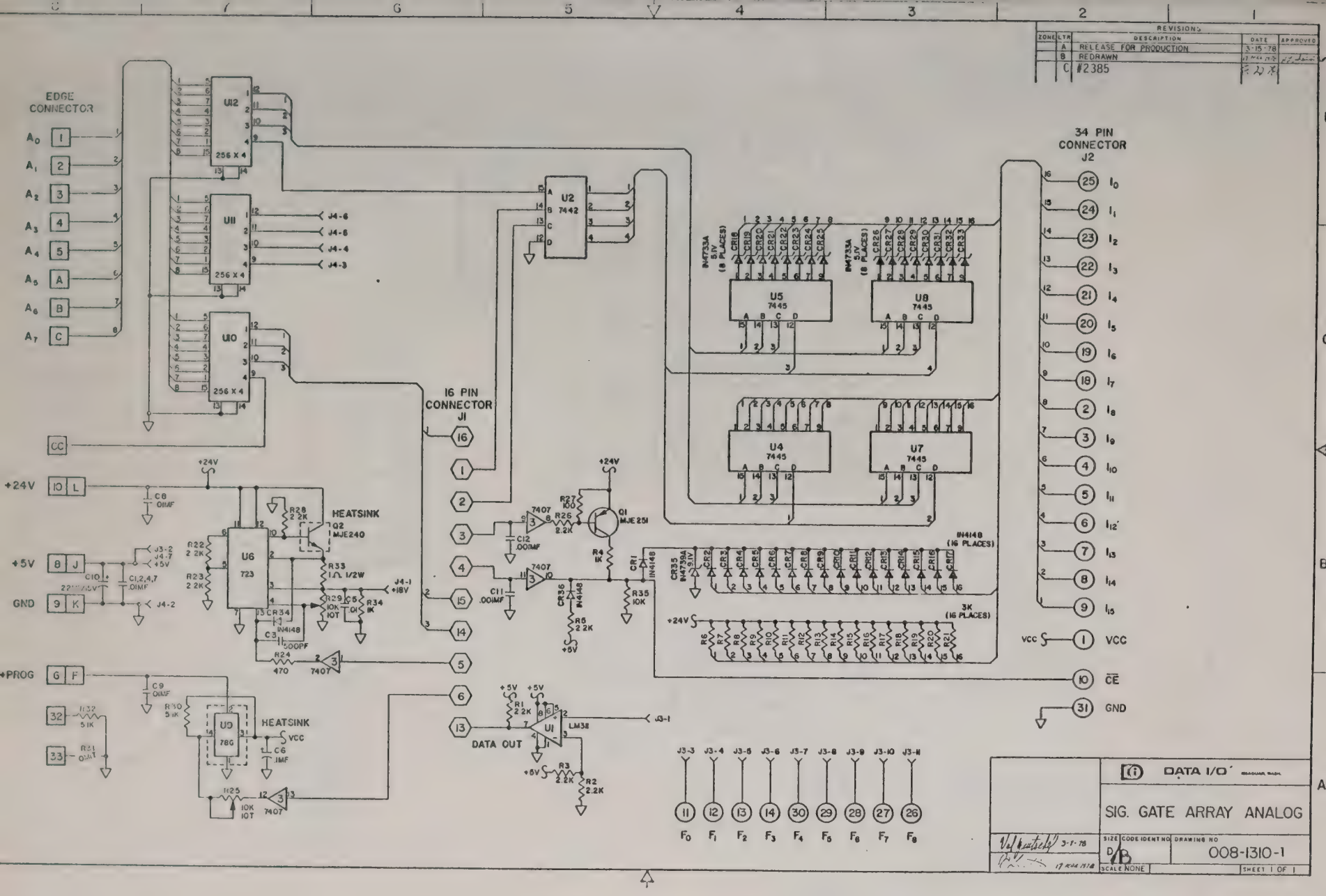
CONTROL ROM U5

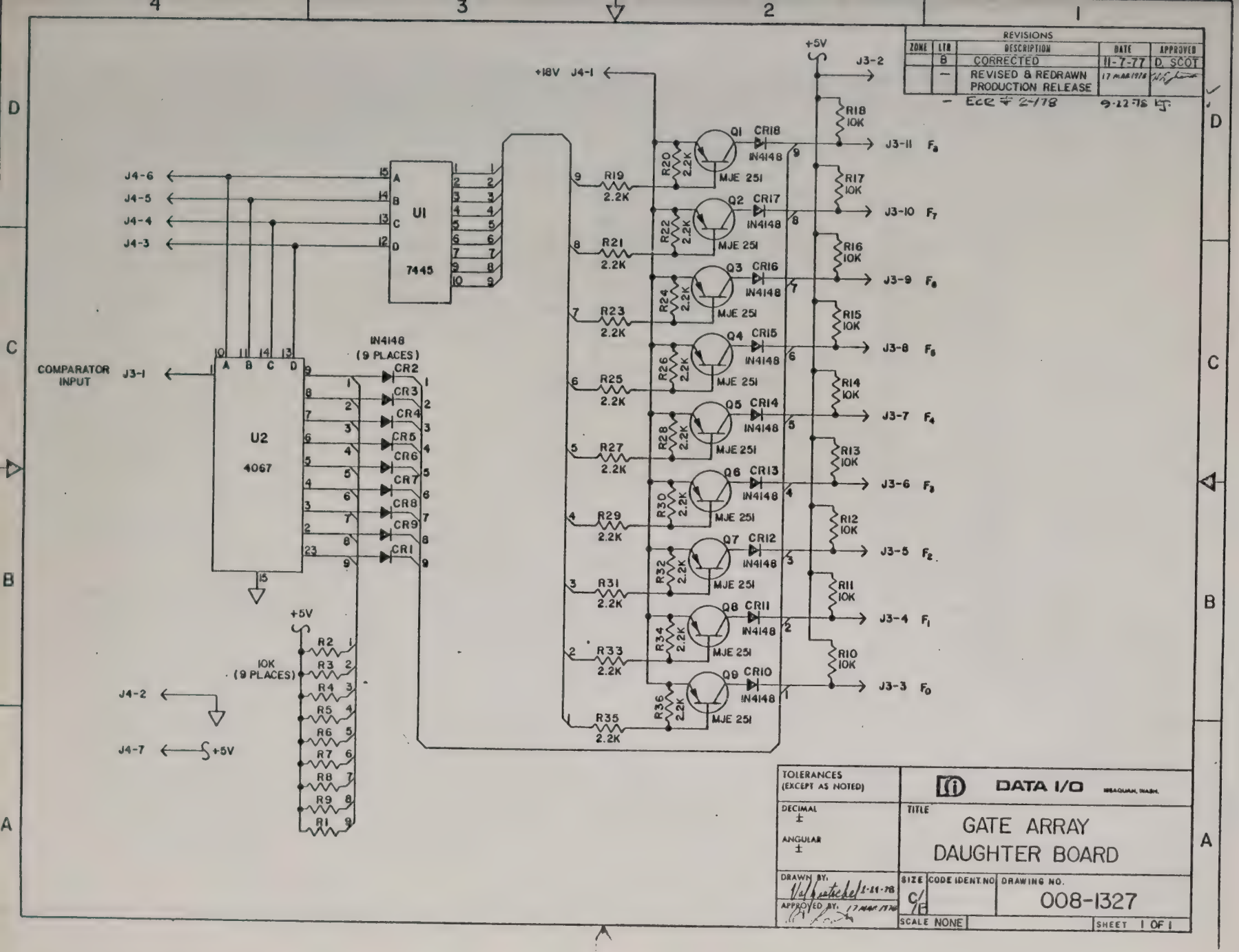


DATA I/O ISSAQUAH, WASH.

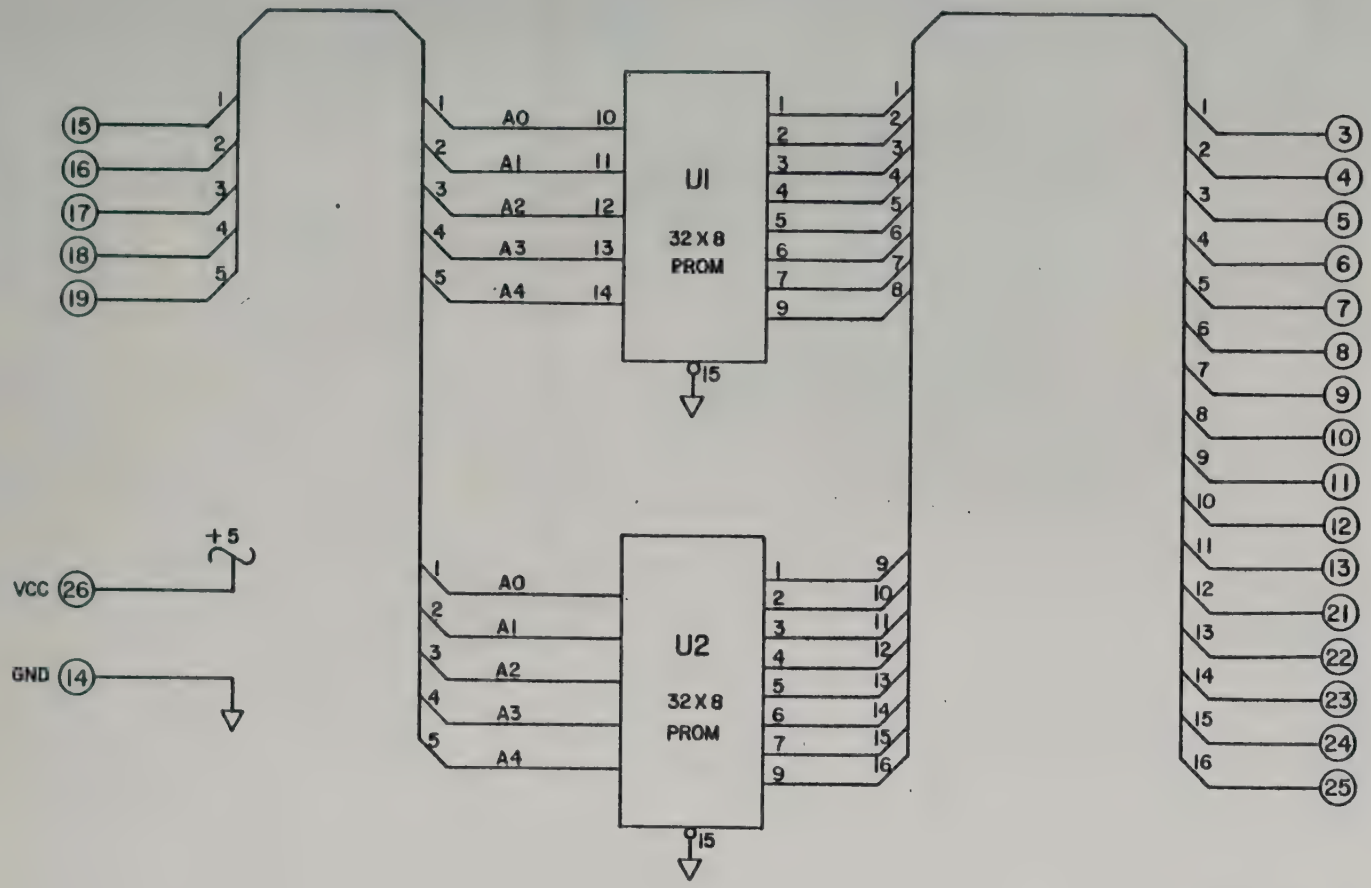
SIGNETICS GATE ARRAY	DRAWN BY G. J.
	APPROVED BY
TITLE: TIMING DIAGRAM	Sheet 2 of 2
DATE: 3-1-77	DRAWING NUMBER: 007-1310-1


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A PROTOTYPE RELEASE 3-77 G JAMES
B CORRECTED 11-77 G JAMES
— REDRAWN 2-78 G JAMES
C ECN# 2387 8-24-78 G JAMES
DI REGISTER
DO REGISTER
PROG MEM
MASTER CLOCK
WORD SKIP
O = PROG
MODE CONTROLLER
NAND BIT MEM
TIMING SEQ.
ABORT
ABORT COUNTER
ABORT TIMER
DATA I/O
GATE ARRAY DIGITAL
DRAWING NO 008-1309
SIZE D/8
SCALE NONE
SHEET 1 OF 1


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A RELEASE FOR PRODUCTION 3-15-78
B REDRAWN
C #2385
EDGE CONNECTOR
34 PIN CONNECTOR J2
16 PIN CONNECTOR J1
U12 256 X 4
U11 256 X 4
U10 256 X 4
U2 7442
U5 7445
U8 7445
U4 7445
U7 7445
U6 723
U9 78G
U1 LM311
Q1 MJE251
Q2 MJE240
HEATSINK
DATA OUT
+24V
+5V
GND
+PROG
VCC
CE
DATA I/O
SIG. GATE ARRAY ANALOG
008-1310-1
SIZE D
SCALE NONE
SHEET 1 OF 1


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B | CORRECTED | 11-7-77 | D. SCOT
– | REVISED & REDRAWN PRODUCTION RELEASE | 17 MAR 1978
– ECO # 2-178 9-22-78
+5V
+18V J4-1
J3-2
J4-6
J4-5
J4-4
J4-3
U1
7445
IN4148 (9 PLACES)
COMPARATOR INPUT J3-1
U2
4067
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR1
10K (9 PLACES)
R2
R3
R4
R5
R6
R7
R8
R9
R1
J4-2
J4-7
+5V
R19 2.2K
R21 2.2K
R23 2.2K
R25 2.2K
R27 2.2K
R29 2.2K
R31 2.2K
R33 2.2K
R35 2.2K
R20 2.2K
R22 2.2K
R24 2.2K
R26 2.2K
R28 2.2K
R30 2.2K
R32 2.2K
R34 2.2K
R36 2.2K
Q1 CR18 IN4148 MJE 251
Q2 CR17 IN4148 MJE 251
Q3 CR16 IN4148 MJE 251
Q4 CR15 IN4148 MJE 251
Q5 CR14 IN4148 MJE 251
Q6 CR13 IN4148 MJE 251
Q7 CR12 IN4148 MJE 251
Q8 CR11 IN4148 MJE 251
Q9 CR10 IN4148 MJE 251
R18 10K
R17 10K
R16 10K
R15 10K
R14 10K
R13 10K
R12 10K
R11 10K
R10 10K
J3-11 F8
J3-10 F7
J3-9 F6
J3-8 F5
J3-7 F4
J3-6 F3
J3-5 F2
J3-4 F1
J3-3 F0
TOLERANCES (EXCEPT AS NOTED)
DECIMAL ±
ANGULAR ±
DRAWN BY: 2-26-78
APPROVED BY: 17 MAR 1978
DATA I/O REDMOND, WASH.
TITLE
GATE ARRAY DAUGHTER BOARD
SIZE C/B
CODE IDENT. NO
DRAWING NO. 008-1327
SCALE NONE
SHEET 1 OF 1

DATE	BYM	REVISION RECORD	DR	CK
11-18-75	A	RELEASE		



TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL ±		SCALE	DRAWN BY G. ROPPE
FRACTIONAL ±	TITLE PLUG IN ADAPTER (UNIVERSAL CALIBRATOR)		APPROVED BY
ANGULAR ±	DATE 10-15-75	DRAWING NUMBER 008-1072	

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Programming systems for tomorrow...today

Reader Comments

The manual's completeness, accuracy, organization, usability, and reliability: _____

_____

Did you find errors in this manual: _____

How can this manual be improved: _____

_____

_____

Additional comments: _____

_____

Name _____

Company _____ Department _____ M/S _____

Address _____

City _____ State _____ Zip _____ Phone _____

Manual or Part No. _____

Warranty/Registration

Please return this card to Data I/O within five days

Did the packaging of this equipment exhibit any outward signs of physical damage? . . . . . YES ○ ○ NO
Did this equipment arrive intact, without loose parts or cable damage? . . . . . YES ○ ○ NO
Did the equipment operate on power-up?. . . . . YES ○ ○ NO
Did you attain adequate system performance? . . . . . YES ○ ○ NO
Were any electrical adjustments required? . . . . . YES ○ ○ NO
If you required assistance, was a local Data I/O representative contacted? . . . . . YES ○ ○ NO

Comments – _____

_____

Name _____ Title _____

Department _____ M/S _____

Company _____

Address _____

City _____ State _____ Zip _____ Phone ( ) _____

Model or Description _____ Serial or Part No. _____

Date Received _____

90 Day Warranty

Data I/O warrants that all equipment sold pursuant to any resultant agreement shall be free from defects in material or workmanship at the time of delivery. Such warranty shall extend for 90 days. Buyer must provide notice to Data I/O within this prescribed warranty period of any defect; if the defect is not the result of improper usage, service, maintenance or installation and equipment has not been otherwise damaged or modified after delivery, Data I/O shall either replace or repair the defective part or parts of equipment or replace the equipment or refund the purchase price at Data I/O's option after return of such equipment by buyer to Data I/O. Shipment to and from Data I/O's facility shall be borne on account of buyer.

(a) Consequential Damages — Data I/O shall not be liable for any incidental or consequential damages incurred as a result of any defect in any equipment sold hereunder and Data I/O's liability is specifically limited to its obligation described herein to repair or replace a defective part or parts covered by this warranty.

(b) Exclusive Warranty — The warranty set forth herein is the only warranty, oral or written made by Data I/O and is in lieu of and replaces all other warranties, expressed or implied, including the WARRANTY OF MERCANTIBILITY AND THE WARRANTY OF FITNESS FOR PARTICULAR PURPOSE.

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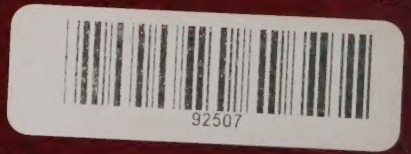
DATA I/O Warranty/Registration

Service Manager
P. O. Box 308
1297 Northwest Mall
Issaquah, WA 98027



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